Functionality-Enhanced Devices
An Alternative to Moore's Law

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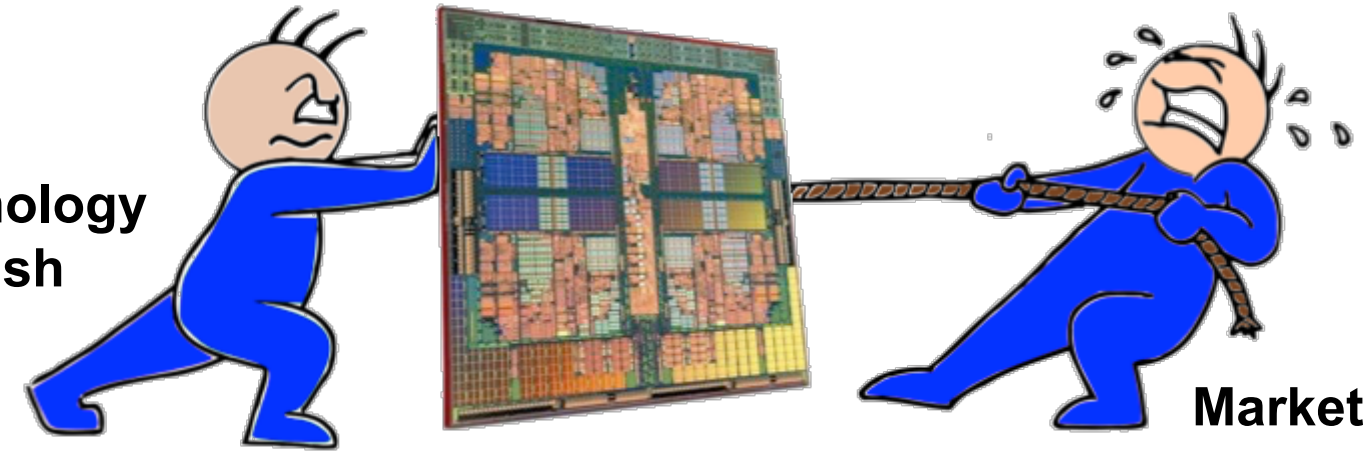
An Alternative to Conventional Scaling

Traditional Approach
(supported by dimension scaling)



"Increase the numbers of devices per area unit"

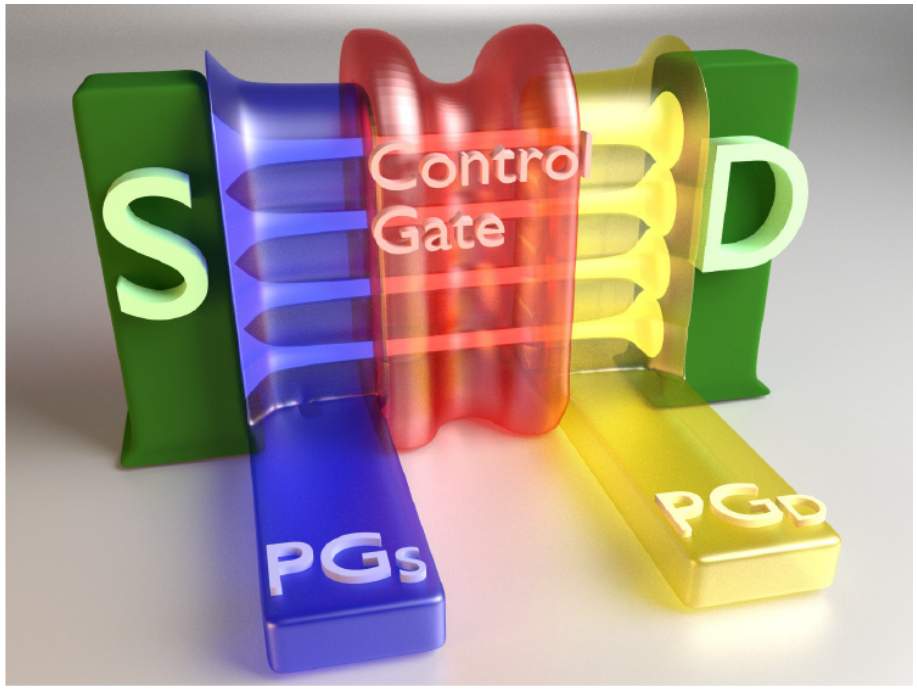
Our Approach
(additional functional scaling)

"Increase the device capabilities for a given area"

Functionality-Enhanced Devices

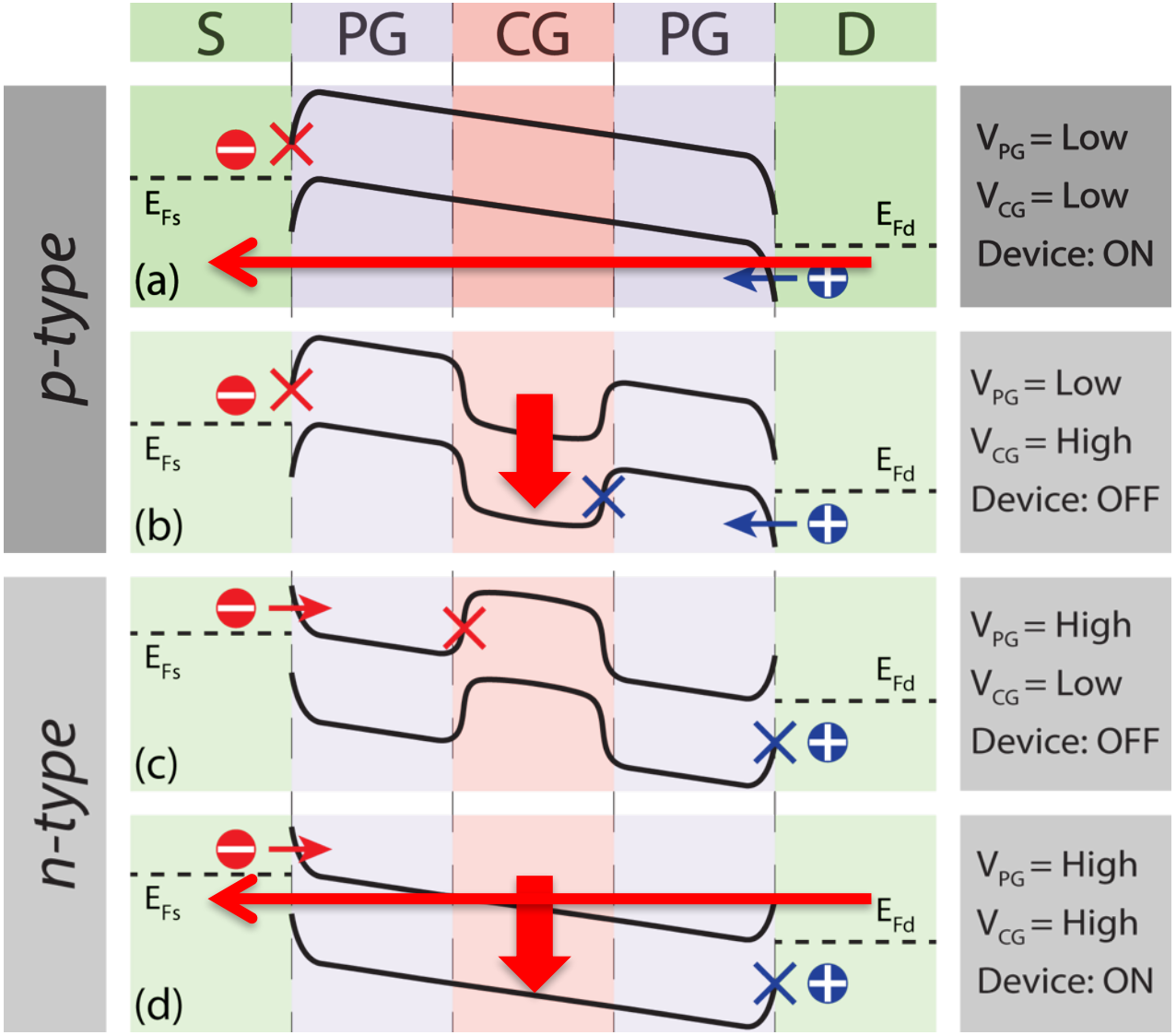
Three-Independent-Gate (TIG) FETs

One device
3 modes of operation
(depending on the different gate polarizations)



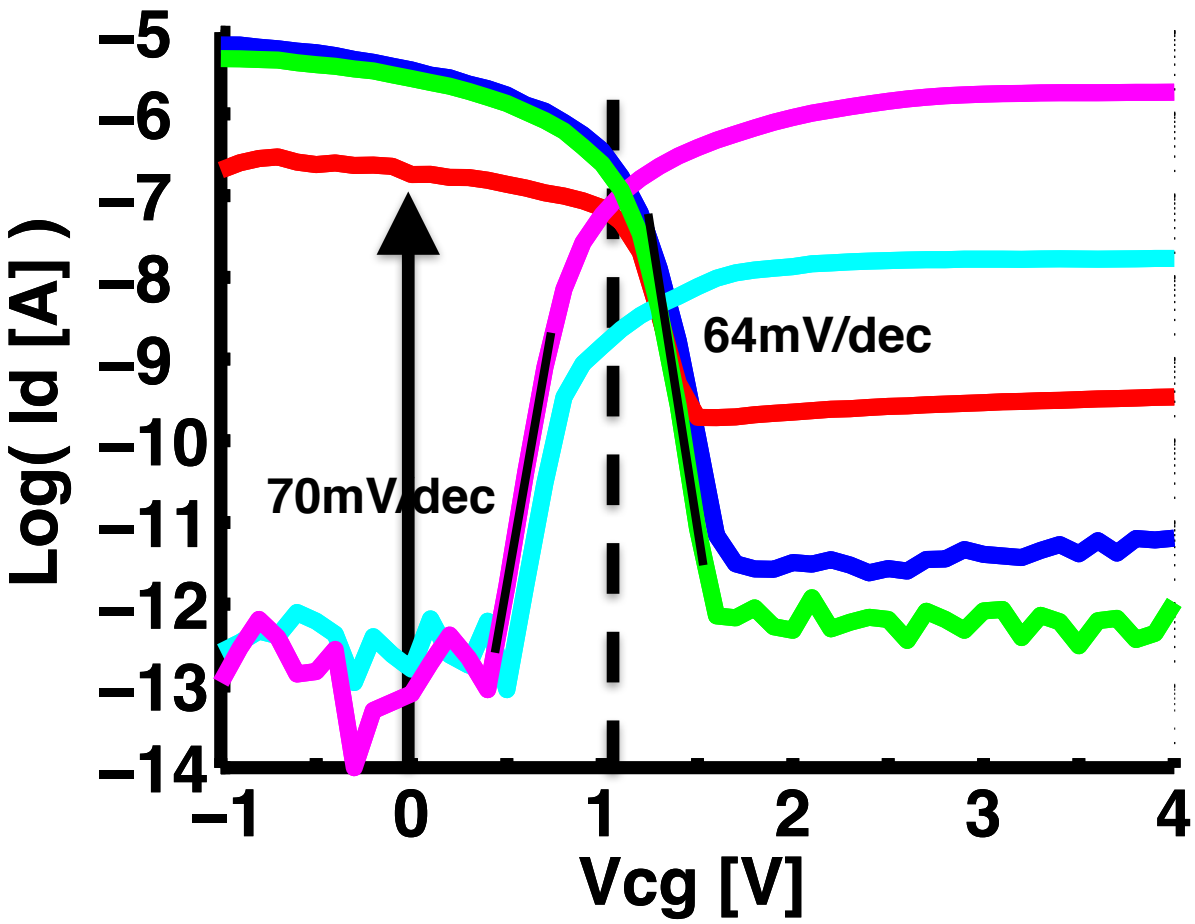
A- Dynamic reconfiguration of the device polarity
B- Dynamic control of the threshold voltage
C- Dynamic control of the subthreshold slope

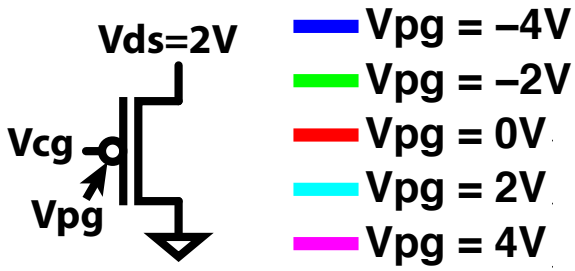
Polarity Control: Working Principle



M. De Marchi *et al.*, *IEDM'12, TNANO'13*

Polarity Control: Measured I_D-V_{CG}





Crossing > 0 V

V_{PG} = 0 V → *p*-type

Symmetry

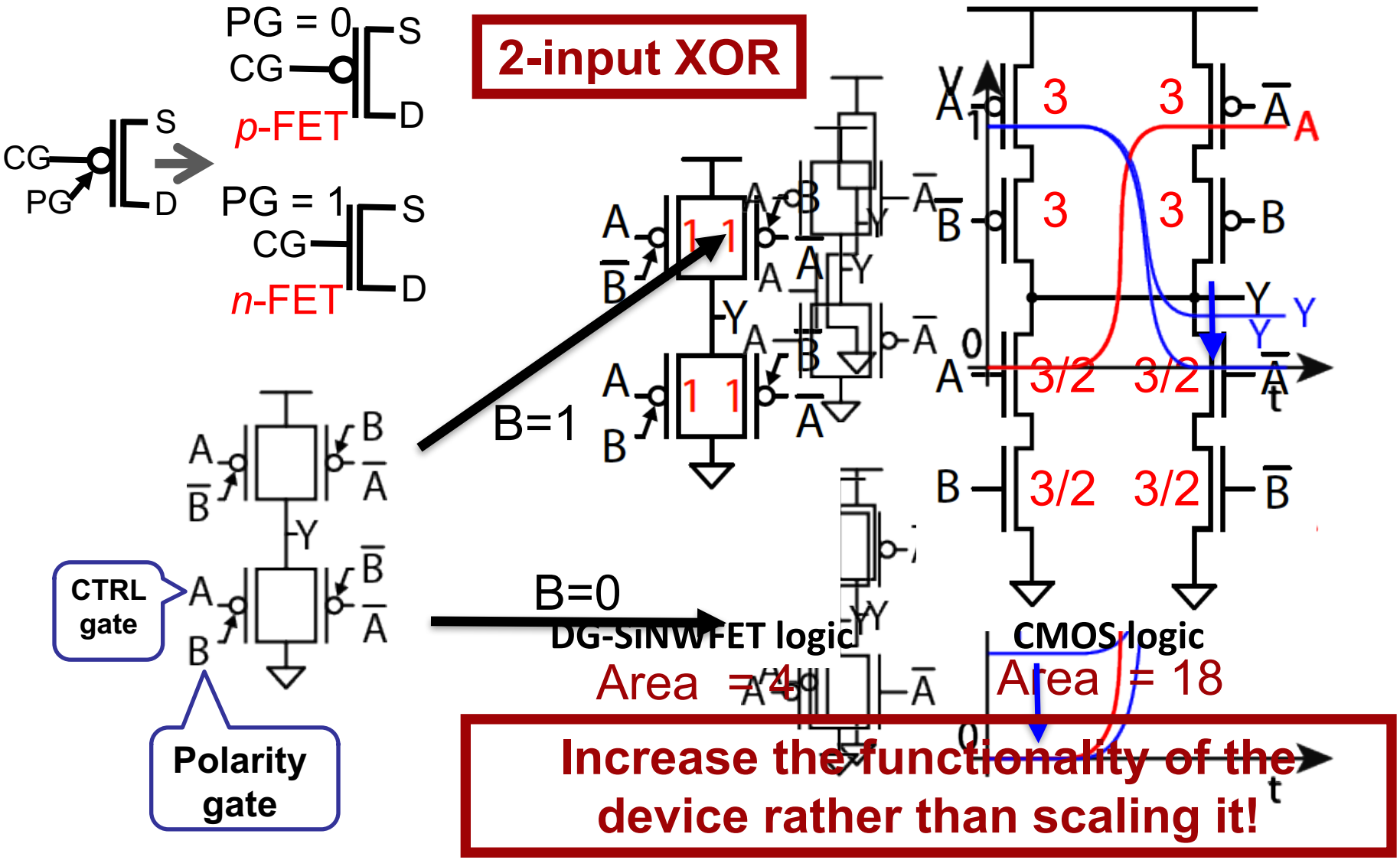
BC: $I_{ON}/I_{OFF} > 10^7$

BC: SS~60 mV/dec

I_{OFF} < 100fA

M. De Marchi *et al.*, *IEDM'12, TNANO'13*

An Extension to Moore's Law

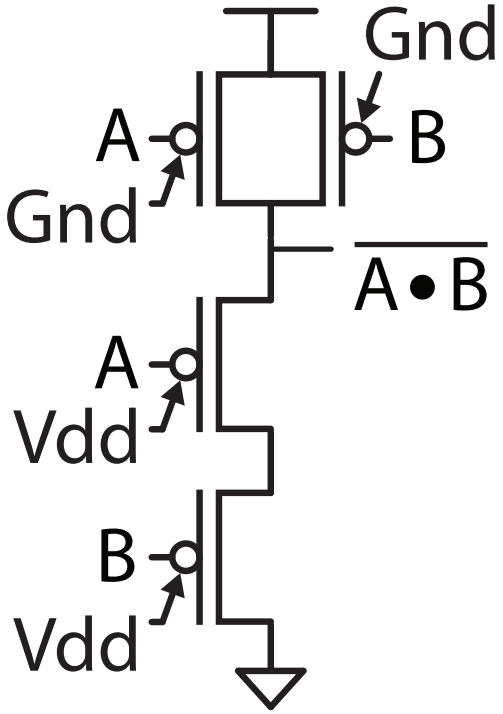


Circuit Design with Controllable-Polarity Transistors

Negative Unate functions

NAND, NOR, AOI, OAI,..

Bias the polarity gates!
(unipolar behavior)

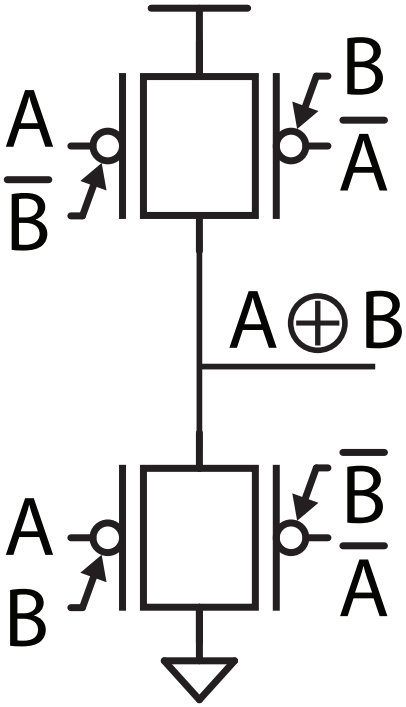


2-input NAND

Binate functions

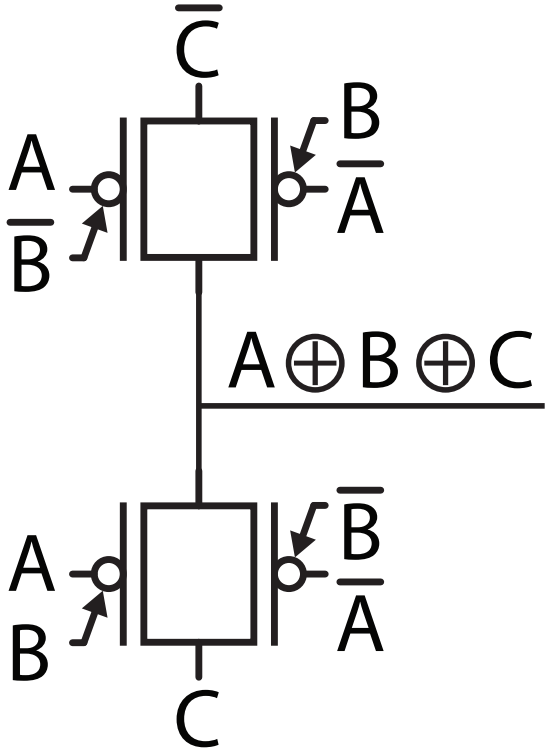
XOR, XNOR,..

Inputs to the polarity gates!
(Exploit the device behavior)



2-input XOR

H. Ben Jamaa *et al.*, *DATE'09*

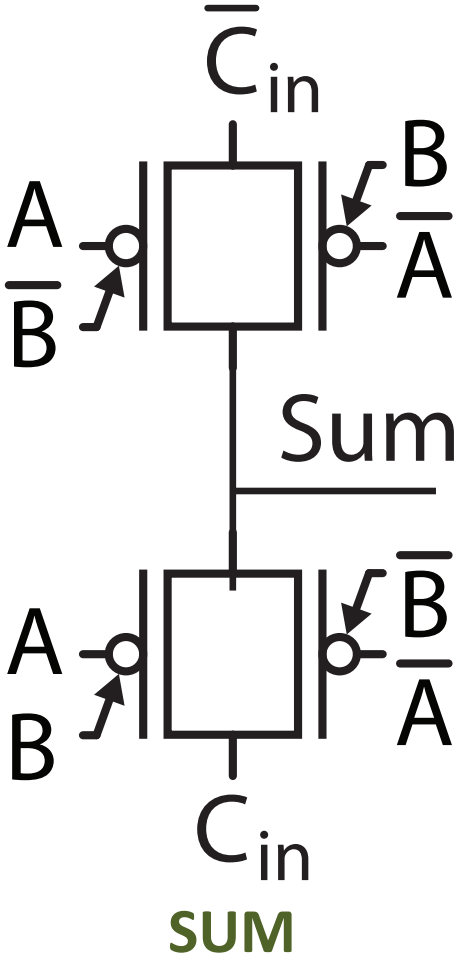


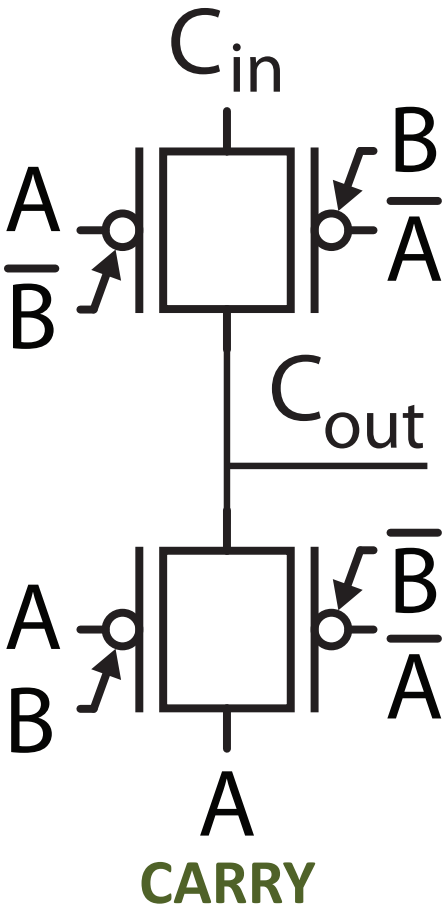
3-input XOR

A. Zukovski *et al.*, *DAC'11*

Compact *Full-Adder* implementation

$$Sum = A \oplus B \oplus C_{IN} \qquad C_{OUT} = MAJ(A, B, C_{IN})$$





8 Transistors

Area saving

(smaller gates)

Delay saving

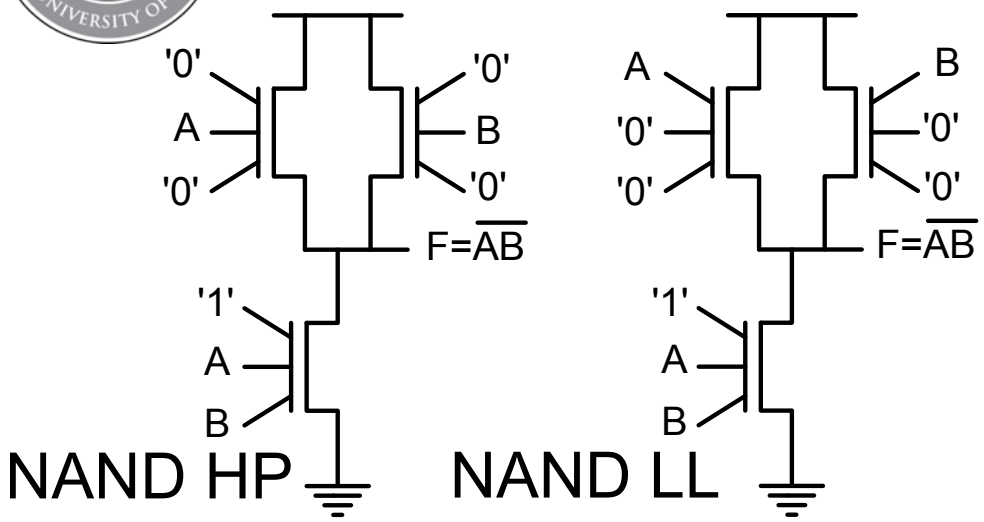
(smaller stacks)

Compact computation primitives

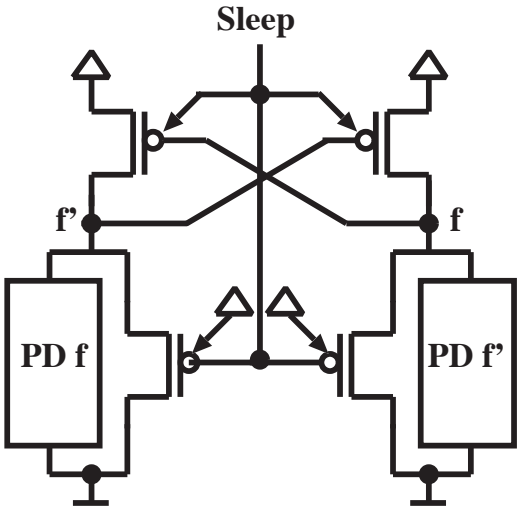
XOR - MAJ

O. Turkyilmaz *et al.*, *ISCAS'13*

Many other circuits !

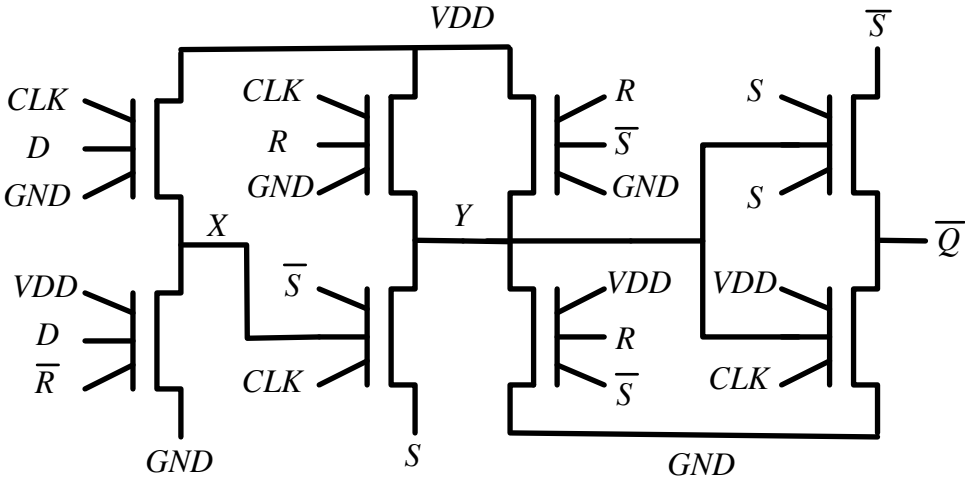


J. Zhang *et al.*, *TCAS-I'14*



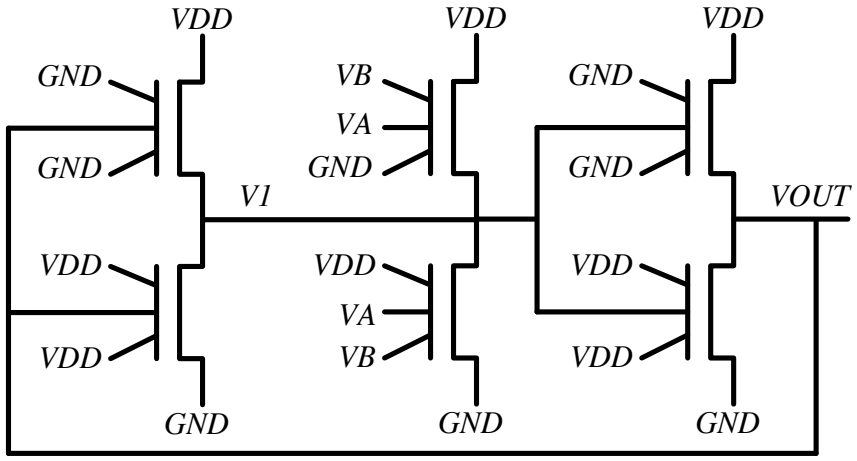
Embedded power gating

L. Amaru *et al.*, *TCAS-I'13*



TSPC Flip Flop

X. Tang *et al.*, *ISCAS'14*



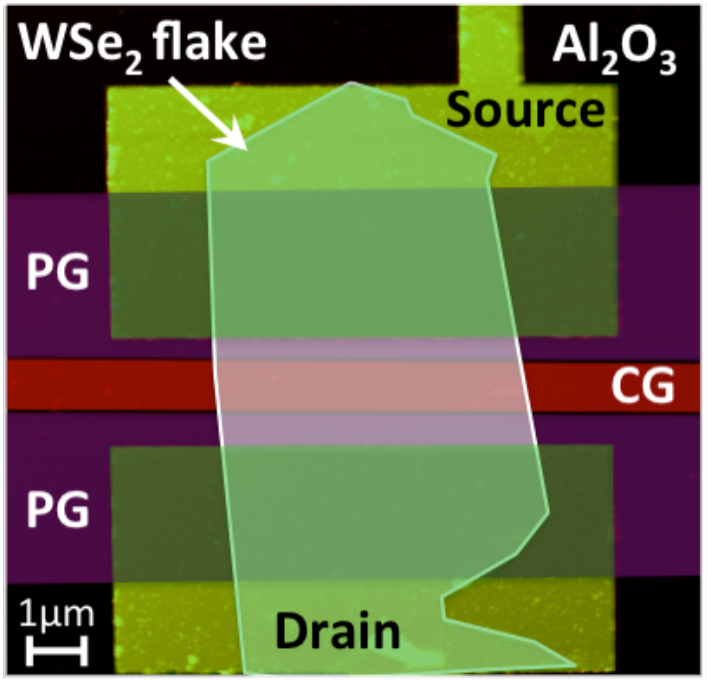
C-Element

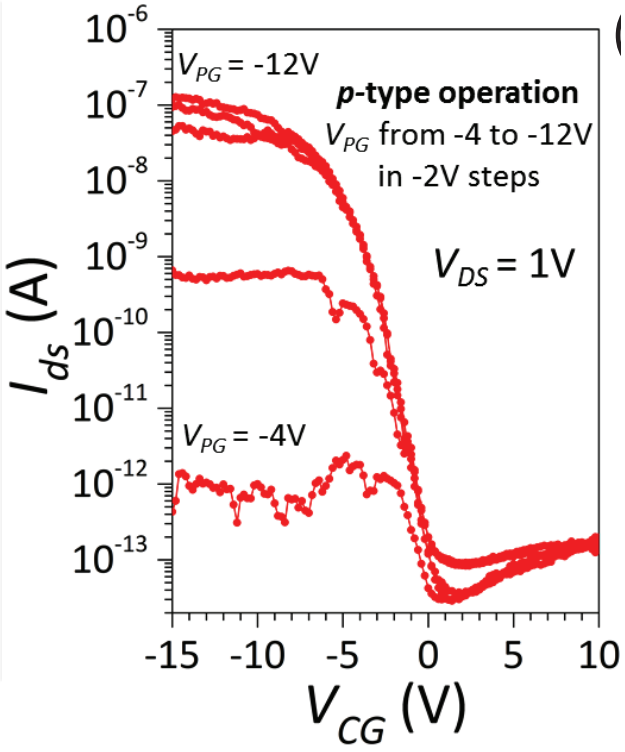
P.-E. Gaillardon *et al.*, *LATS'16*

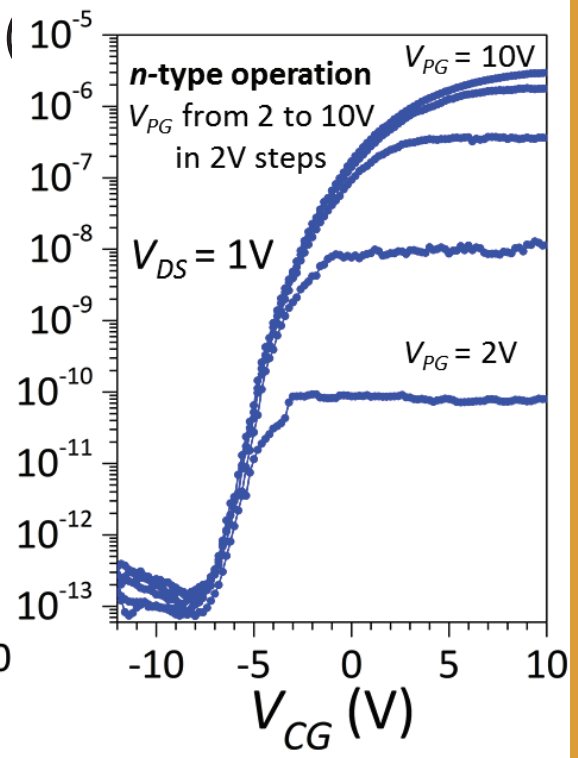
Recent Validation of TMD Materials

Interesting concept for 2D material

(arguably difficult to make unipolar)





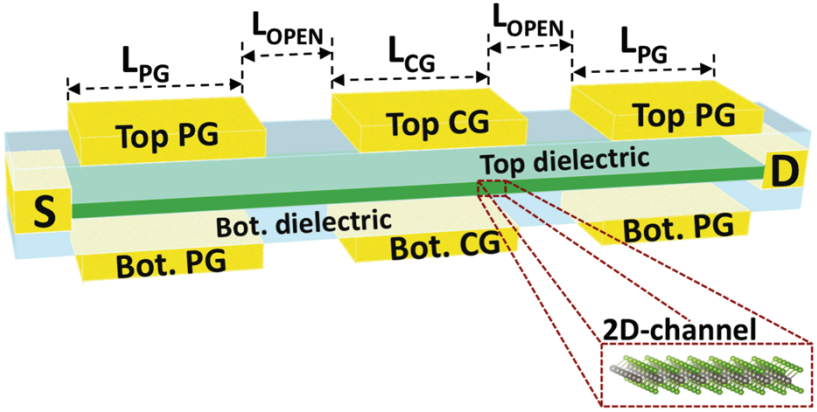


Proven ambipolarity in WSe_2

$I_{ON}/I_{OFF} > 10^6$

G. Resta *et al.*, *Scientific Reports'16*

Performances at Advanced Scaling



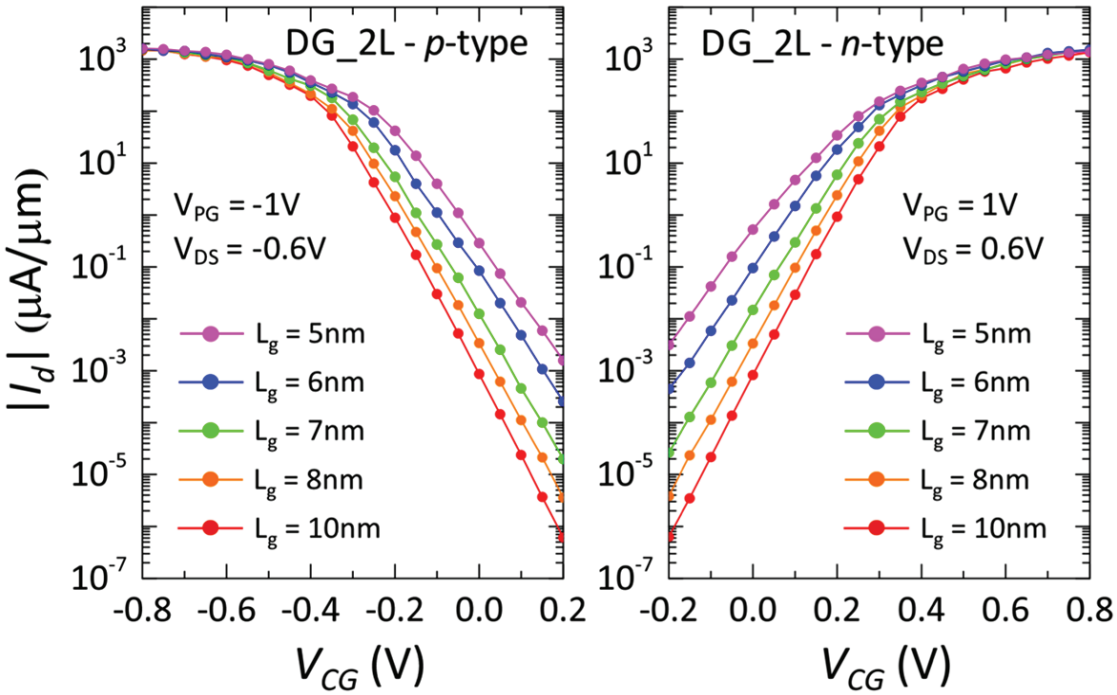
Quantum simulations using NanoTCAD ViDES

2-layer TMD (0.8eV)
Bottom and Top gates
Scaled HfO_2

At L_G = 5nm,

TMD TIGFETs
J_{on} = 1.5 mA/μm
J_{off} = 10^{-2} μA/μm

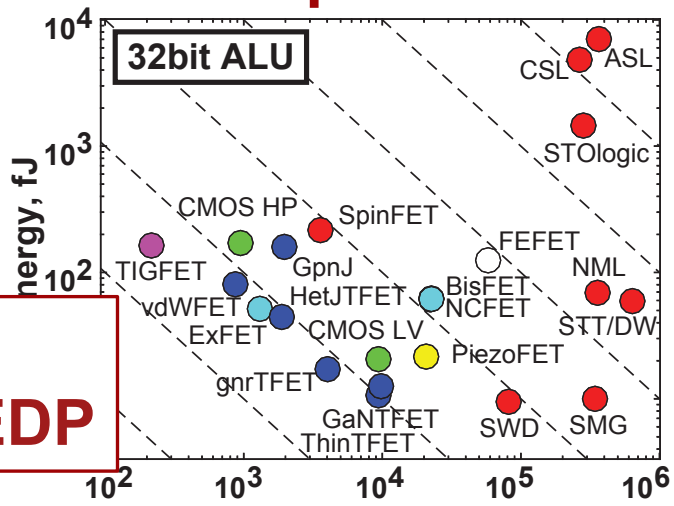
CMOS [ITRS2013]
J_{on} = 0.9 mA/μm
J_{off} = 0.1 μA/μm



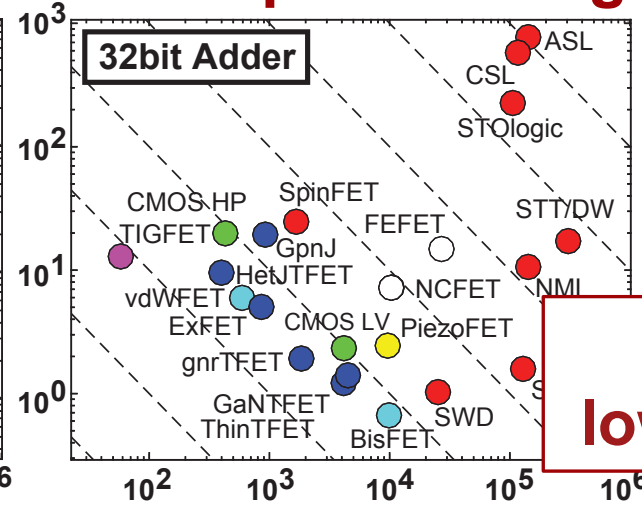
G. Resta *et al.*, *Scientific Reports'16*

Evaluation at BCB level

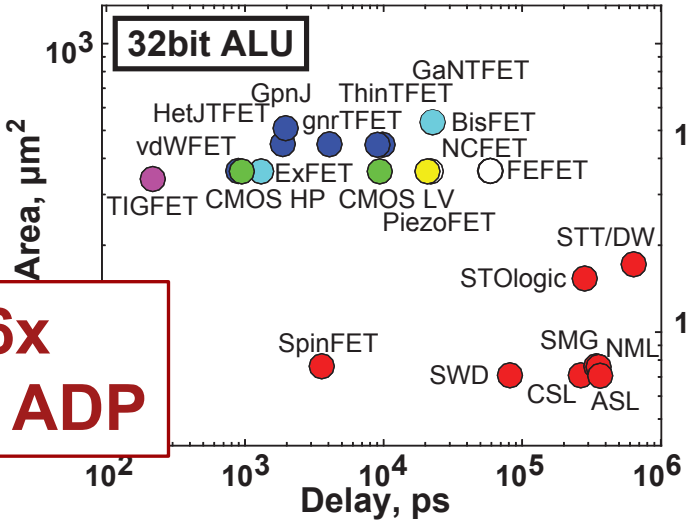
What is the effect of TMD-TIGFET device performance coupled with TIGFET superior design?



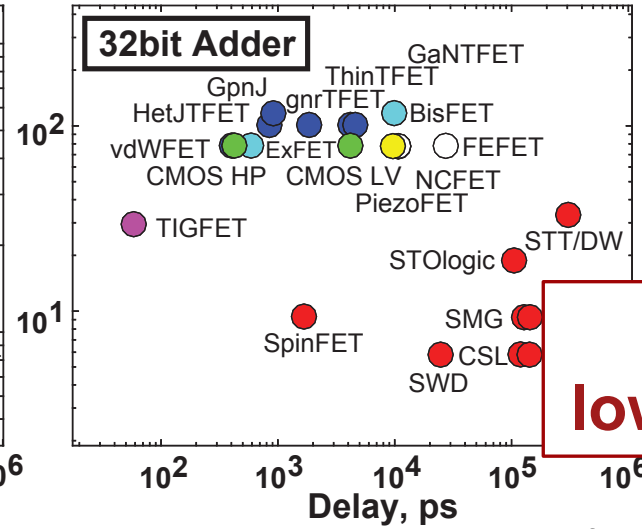
4.5x lower EDP



11.2x lower EDP



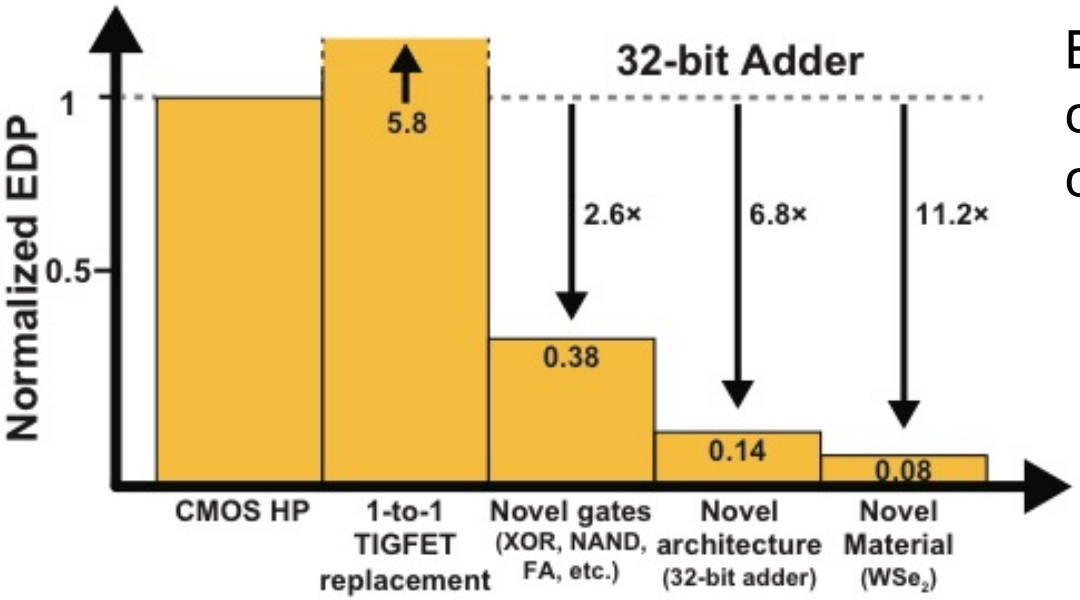
4.6x lower ADP



14.4x lower ADP

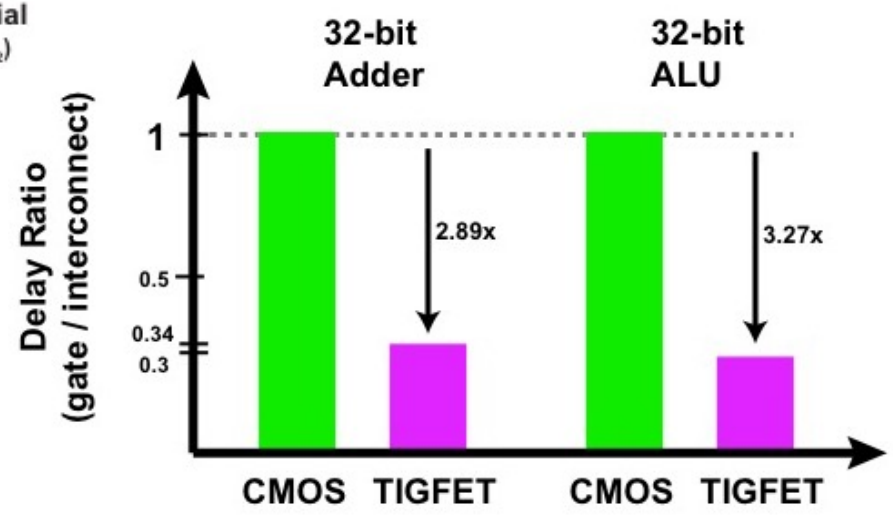
unpublished

Origin of the Benefit



Benefits do come from the capability of TIGFETs to realize compact gates and systems.

TIGFETs compactness leads to less interconnect parasitics to drive.



unpublished

Why EDA must follow Emerging Techs?

- Logic Synthesis (and EDA) is a **CMOS supporter**
  - LS techniques derive from CMOS abilities - NAND/NOR/MUX
  - Novel technologies and computing paradigms disrupt this model
- Logic Synthesis may evolve towards **more expressive primitives**, i.e., **MAJ-based Logic** and be **more technology-aware**

More expressive CMOS
L. Amarù *et al.*, *TCAD'16*

Nanotechnologies (RRAMs, SWD,…)
E. Testa et al., Nanoarch'16* - S. Shirinzadeh *et al.*, *DATE'16* - P.-E. Gaillardon et al., *DATE'16

Neuromorphic computing (threshold)

Donald E. Knuth (The Art of Computer Programming – 4A): "**MAJ(x,y,z) is probably the most important ternary operation in the entire universe**, because it has amazing properties that are continually being discovered and rediscovered."

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Mr. Gain Kim
Mr. Edouard Giacomin

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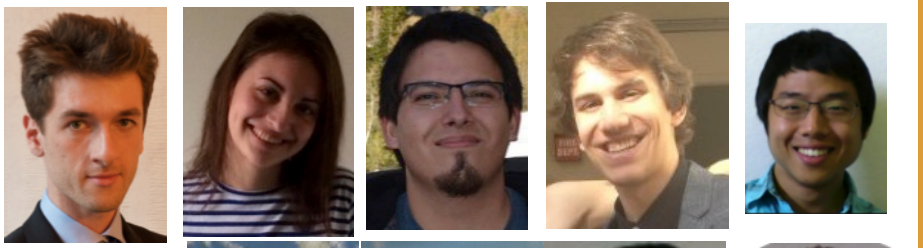
Ms. Eleonora Testa

Physical Design

Modeling



Technology

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Thank you for your attention

Questions?

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